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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/883,681	06/18/2001	Ashok Singhal	M-8496 US	1044

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,681	SINGHAL ET AL.	
	Examiner	Art Unit	
	Nimesh G. Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-14,16,18,19 and 21-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-14,16,18,19 and 21-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-7, 9-13, 14, 16, 18-19 and 24-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al.(5,642,478), hereinafter referred to as Chen.

3. Regarding claim 1, Chen discloses a node controller(Figure 1, 38) for a node(Figure 1, 16) in a data storage system, the node being linked to another node(Figure 1, 18) and the nodes being coupled to a same host device(Figure 1, 12) and same storage device(Figure 1, 26), each node comprising one computer-memory complex(Figure 1, 30) and one node controller(Figure 1, 38) distinct from said one computer-memory complex, the node controller being operable to transfer data between the two nodes as instructed by a computer-memory complex of the node but without any further intervention by the computer-memory complex, the node controller comprising a cluster memory(Figure 1, 32) for storing data being transferred between the two nodes.

4. Regarding claim 28, Chen discloses a node controller, wherein the node controller comprises a logic engine operable to perform a logic operation on data from at least one data source in the data storage system and to write a result of the logic operation to at least one data destination in the data storage system(Figure 2, 52; Column 7, Lines 63-66).

5. Regarding claim 3, Chen discloses a node controller, wherein at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory(Figure 1).

6. Regarding claim 4, Chen discloses a node controller, wherein the logic engine comprises an exclusive OR engine(Column 7, Lines 63-66; XOR operations are used to calculate ECC).

7. Regarding claim 5, Chen discloses a node controller comprising a command queue operable to store a logic control block to be processed by the logic engine, the logic control block specifying said at least one data source and said at least one data destination(e.g. Column 8, Lines 57-67).

8. Regarding claim 6, Chen discloses a node controller comprising a memory controller operable to interface with a cluster memory(e.g. Column 7, Lines 63-66).

9. Regarding claim 7, Chen discloses a node controller, wherein the node controller is implemented as an integrated circuit device(e.g. Figure 2, 38).

10. Regarding claim 9, Chen discloses a node controller(Figure 1, 38) for a node(Figure 1, 16) in a data storage system, the node being linked to another node(Figure 1, 18) and the nodes being coupled to a same host device(Figure 1, 12) and same storage device(Figure 1, 26), each node comprising one computer-memory complex(Figure 1, 30) and one node controller(Figure 1, 38) distinct from said one computer-memory complex, the node controller comprising: a plurality of logic engines operable to perform a logic operation on storage data originating from at least one data source in the data storage system and to write a result of the logic operation to at least one data destination in the data storage system, the logic engine performing the logic operation as instructed by a computer-memory complex of the node but without further intervention by the computer-memory complex; and command queues coupled to the logic engines, the command queues operable to store logic control blocks which can be processed by the logic engines(e.g. Column 8, Lines 57-67).

11. Regarding claim 10, Chen discloses a node controller, wherein at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory(Figure 1).

12. Regarding claim 11, Chen discloses a node controller, wherein the logic engine comprises an exclusive OR engine(Column 7, Lines 63-66; XOR operations are used to calculate ECC).

13. Regarding claim 12, Chen discloses a node controller comprising a command queue operable to store a logic control block to be processed by the logic engine, the logic control block specifying said at least one data source and said at least one data destination(e.g. Column 8, Lines 57-67).

14. Regarding claim 13, Chen discloses a node controller comprising a memory controller operable to interface with a cluster memory(e.g. Column 7, Lines 63-66).

15. Regarding claim 14, Chen discloses a node controller, wherein the node controller is implemented as an integrated circuit device(e.g. Figure 2, 38).

16. Regarding claim 16, Chen discloses a producer register operable to specify a first address of a command queue and a consumer register operable to specify a second address of a command queue (e.g. Column 8, Lines 57-67).

17. Regarding claim 18, Chen discloses a node controller(Figure 1, 38) for a node in data storage system having at least two nodes, each node comprising one computer-memory complex and one node controller distinct from said one computer-memory complex(Figure 1, 30), the node controller comprising: a memory controller(e.g. Column 7, Lines 63-66) for coupling to memory and a backplane, wherein the backplane can be coupled to a plurality of other node controllers in the data storage system; a plurality of input/output interfaces for coupling to a computer-memory complex of the node, a host device(Figure 1, 12), and a storage device(Figure 1, 26) all on a plurality of buses; a plurality of logic engines coupled to (1) the memory controller (2) the backplane, and (3) the plurality of input/output interfaces; wherein in a first type of data transfer, one of the logic engines performs a logic operation to a plurality of storage data from one of a plurality of data sources in the data storage system and writes the result of the logic operation to one of a plurality of data destinations in the data storage system, the data sources comprising the cluster memory and the input/output interfaces, and the data destinations comprising, the cluster memory, the backplane, and the input/output interfaces(e.g. Column 7, Lines 49-54 and 63-66).

18. Regarding claim 19, Chen discloses a node controller, wherein, in a second type of data transfer, one of the data sources writes a data into the memory and in response one of the logic engine copies the data to at least one of the data destinations(e.g. Column 7, Lines 49-54 and 63-66).

19. Regarding claim 20, Chen discloses a node controller, wherein each of the devices is selected from the group consisting of a host device and a data storage device(Figure 1).

20. Regarding claim 24, Chen discloses a node controller, wherein the computer-memory complex is not burdened with temporarily storing data being transferred thorough the node in the computer-memory complex(e.g. Column 7, Lines 49-54).

21. Regarding claim 25, Chen discloses a node controller, wherein the logic operation comprises an XOR operation(e.g. Column 7, Lines 63-66, XOR operations are used to calculate ECC).

22. Regarding claim 26, Chen discloses a node controller, wherein the XOR operation is used to calculate a parity data for writing a full or a partial RAID stripe(e.g. Column 7, Lines 63-66).

23. Regarding claim 27, Chen discloses a node controller, wherein the XOR operation is used to reconstruct a lost data using a parity(e.g. Column 7, Lines 63-66).

24. Regarding claim 29, Chen discloses a node controller(Figure 1, 38) for a first node(Figure 1, 16) in a data storage system comprising at least the first node and a second node(Figure 1, 18), each node comprising one computer-memory complex(Figure 1, 30) and one node controller distinct from said one computer-memory complex, the node controller comprising: a memory controller(Figure 2, 52) for accessing a cache memory of the first node; one or more bus interfaces for communicating with a host device(Figure 1, 12), a data storage device(Figure 1, 26), and the computer-memory complex all located on one or more buses; a link to a second node(Figure 1, 24); wherein in a first type of data transfer: the computer-memory complex instructs the data storage device to write data into the memory; the data storage device writes the data into the memory via one or more buses; the computer-memory complex

instructs the node controller to send the data to the second node; and the node controller sends the data to the second node via the link(e.g. Column 7, Lines 49-54 and 63-66).

25. Regarding claim 30, Chen discloses a node controller, further comprising: a logic engine; wherein in a second type of data transfer: the computer-memory complex instructs the node controller to perform a logic operation to a plurality of data in the memory; the node controller uses the logic engine to perform the logic operation to the plurality of data(e.g. Column 7, Lines 63-66).

26. Regarding claim 31, Chen discloses a node controller, wherein the second type of data transfer further comprises: the computer-memory complex instructs the node controller to send a result of the logic operation to the second node; and the node controller sends the result to the second node via the link (e.g. Column 7, Lines 49-54 and 63-66).

27. Regarding claim 32, Chen discloses a node controller; wherein in a third type of transfer: the computer-memory complex instructs the data storage device to write the data into the memory; the data storage device writes the data into the memory via the one or more buses; the computer-memory complex instructs the host device to read the data from the memory; and the host device reads the data form the memory via the one or more buses(E.g. Column 7, Lines 49-54 and 63-66).

28. Regarding claim 33, Chen discloses a node controller, wherein at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory(Figure 1).

29. Regarding claim 34, Chen discloses a node controller, wherein at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory(Figure 1).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

32. Claims 8, 14 and 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen, in view of what is well known in the art.

33. Regarding claims 8, 14 and 21, Chen does not specifically disclose a node controller comprising a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus. However, the use of a PCI bus is well known in the art and therefore would have been obvious to one of ordinary skill in the art to use the PCI bus in the system of Chen since it is common bus that is extensively used in the industry..

34. Regarding claim 22, Chen discloses a node controller, wherein the computer-memory complex manages the PCI bus(It is inherent the PCI bus is managed by the computer-memory complex).

35. Regarding claim 23, Chen does not specifically disclose a node controller wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service. However, these services are well known in the art(HTTP is used for internet, NFS is a standard used for providing file system mounts among Unix systems, and CFSI is the new proposed standard for an Internet File System) and would be obvious to use the computer-memory complex for such services since these services use a network of computers or nodes. (The well-known in the art

statement in the previous office action is taken to be admitted prior art because applicant either failed to traverse the examiner's assertion of official notice (see MPEP 2144.03 (C)).

Response to Arguments

36. Applicant's arguments with respect to claims 1, 3-14, 16, 18-19 and 21-34 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
12/27/05

NP
December 23, 2005